Advanced Computer Architecture

Code-CS- 830

Credit Hours-3+0

Course Description

This module focuses on advanced computer architectures and low-level system software such as pipelined and Multiprocessor systems. The area of computer architecture is undergoing rapid development; it's important to focus not only on what computer architecture are today, but also on why and how they are designed the way they are. This methodology will equip us with a valuable conceptual grounding in the design principles of computer architecture and will help us architect future networks based on sound principles. Towards this end, new research themes that promise to revolutionize computer architecture will be introduced. In this course, we will study the fundamentals of building scalable computer architecture that enable innovation and services. We will go through the thought-process that went into designing the Internet---which is the best example of a computer architecture that has adapted and scaled to changing environment. By the end of the course, the students will be able to: 1) Develop an understanding of the principles upon which the globa l Internet was designed. 2) Develop an understanding of concepts, tools, and terminology necessary for understanding contemporary research topics 3) Have a broad understanding of various advanced research topics in computer architecture

Text Book:

1. **Advanced Computer Architecture: Parallelism, Scalability, programmability**. *Author:* K. Hwang. *Publisher***:** McGraw Hill, 1993. *In addition to the above, the students will be provided with handouts by the lecturer.*

Reference Book:

1. D. Sima, T. Fountain, P. Kacsuk, Advanced Computer Architecture, Addison-Wesley, 1997.
2. H.S. Stone, High-performance Computer Architecture, 3rd edition, Addison-Wesley**,** 1993.
3. J. L. Hennessy and D. A. Patterson, Computer Architecture: A Quantitative Approach, Morgan Kaufmann**,** 1990.
4. Patterson, D. A. and Hennessy, J. L., Computer Organization and Design: The Hardware/ Software Interface, Morgan Kaufmann, 1998.

Learning Outcomes:

- **Knowledge and understanding (CLO-1) (BT Level: C-2, PLO-1)**
  - Understand the advanced concepts of computer architecture.
  - Exposing the major differentials of RISC and CISC architectural characteristics.

- **Cognitive skills (thinking and analysis) (CLO-2) (BT Level: C-4, PLO-2)**
  - Investigating modern design structures of Pipelined and Multiprocessors systems.

- **Communication skills (personal and academic) (CLO-3) (BT Level: C-2, PLO-2)**
  - Become acquainted with recent computer architectures and I/O devices, as well as the low-level language required to drive/manage these types of advanced hardware.

- **Practical and subject specific skills (Transferable Skills) (CLO-4) (BT Level C-4, PLO**
  - Preparing selected reports that imply some emergent topics supporting material essence.

ASSESSMENT SYSTEM FOR THEORY

Mid Semester Exam (MSE)	**30%**
End Semester Exam (written unseen exam)	**40 %**
Reports, Case Studies, Assignments, Research Papers	**30%**
Total	**100%**

Teaching Plan:

Week	Basic and support material to be covered	Homework/reports and their due dates
(1)	*Review of Computer Organization and Architecture.*	

(2)	Computer Architecture: *Computer Components.* *Classification of computer architectures.* *Performance of computer architecture.*	Tutorial 1
(3)	RISC-Architecture: *RISC versus CISC Controversy*. *Characteristics Of RISC-Architectures.*	
(4)	*RISC Pipelining*: *Pipelining with Regular Instructions.* *Optimization of Pipelining.*	Assignment 1
(5)	Processors: *Advanced Processor Technology.* *RICS Scalar Processors.*	
(6)	Memory Hierarchy: *Hierarchical Memory Technology.* *Inclusion, Coherence and Locality.*	Tutorial 2
(7)	*Memory Capacity Planning.* *Cache Memory Organization.* *Cache Addressing* *Models.*	
Mid Semester Exam (MSE)		
(8)	*Vector Processing Principles.* *Vector Processor Model.* *Vector Instruction Types*	Assignment 2
(9)	*Superscalar Processors. VLIW* *Processors.*	
(10)	Buses and Arbitration: *Hierarchical Bus System.* *Backplane Bus Specification.*	Tutorial 3
(11)	*Bus Arbitration and Control.* *Arbitration, Transaction and Interrupt.*	Assignment 3
(12)	Multiprocessor Memory Architectures: *Interleaved Memory Organization.* *Shared-Memory Multiprocessors.* *Distributed-Memory Multiprocessors.*	Project

(13)	Multiprocessor Interconnection Networks: *System Interconnect architecture.* *Network Properties.*	Tutorial 7
(14)	*Interconnection Network Topologies.* *Static Connection Network.* *Dynamic Connection Network.*	
(15) Specimen examination (Optional)	Peripheral Devices: *Disk Arrays.* *Video/Audio Devices.*	Seminar
(16) End Semester Exam	Final Exam Review	Seminar